REMARKS

This Amendment responds to the Office Action mailed November 27, 2007 in the above-identified application. Based on the following comments, careful reconsideration and allowance of the application are respectfully requested.

Claims 1-8, 25 and 27 are currently pending in the application, with claim 1 being the sole independent claim. No claims are amended or canceled. The currently pending claims are listed on the preceding pages for the convenience of the Examiner.

The Examiner has rejected claims 1-3, 7, 25 and 27 under 35 U.S.C. §103(a) as unpatentable over Heath et al. (US 4,901,234) in view of Dowling (US 6,163,836). Claims 4-6 and 8 are rejected under 35 U.S.C. §103(a) as unpatentable over Heath et al. in view of Dowling and Bowes et al. (US 5,655,151). The rejections are respectfully traversed.

Heath discloses a computer system in which peripherals greater in number than the number of DMA channels provided in the system can all have DMA access. Some of the DMA channels are dedicated to certain ones of the peripherals, while others, termed "programmable" DMA channels, are shared by remaining ones of the peripherals (Abstract). A DMA controller 12 is coupled to a system bus 26 and to a family bus 25 (FIG. 1). The details of DMA controller 12 are shown in FIG. 6 of Heath.

Dowling discloses a programmable address arithmetic unit and method for use on microprocessors, microcontrollers and digital signal processors. FIG. 2 of Dowling shows a programmable address arithmetic unit (AAU) 212 and a fixed function AAU 106. An output of one of the AAUs is selected by a MUX 203 and provided to a register set 102. A MUX 122 selects a single address to be provided to data memory 120. FIG. 6 of Dowling discloses a very long instruction word DSP 600 with a first programmable AAU 617 and a second programmable AAU 619 (col. 17, lines 20-23). Addresses to a data memory 658 are provided by a first address multiplexer 650 and a second address multiplexer 652 (col. 17, lines 33-35).

Claim 1 is directed to a DMA controller comprising, in part, at least one peripheral DMA channel, at least one memory DMA stream, first and second address computation units, first and second memory pipelines and a multiplexer. The first and second address computation units

compute updated memory addresses for DMA transfers, wherein the first and second address computation units generate addresses at the same time to permit DMA transfer of data from one memory space to another memory space on the first and second memory access buses. The multiplexer is configured to supply first and second current memory addresses to selected ones of the first and second memory piplines.

The Examiner acknowledges that Heath fails to disclose a controller having first and second address computation units for generating addresses at the same time to permit DMA transfer of data, but asserts that Dowling cures this deficiency (Office Action, page 3). The Examiner refers to Dowling, FIG. 2, elements 212 and 106 as corresponding to the first and second address computation units and to element 122 as corresponding to the multiplexer, as recited by Applicant's claim 1. Applicants must respectfully disagree.

First, it is noted that Dowling relates to a processor having a programmable address arithmetic unit that provides addresses to a data memory 120. The data memory provides data for program execution by a multiply-accumulator 116 (col. 7, lines 60-65). By contrast, Applicant's claims are directed to a DMA controller. As known to those skilled in the art, processors may use direct memory access (DMA) to transfer data from one memory space to another or between a memory space and a peripheral. The processor can request a DMA data transfer and return to normal processing while the DMA controller carries out the data transfer independent of processor activity (page 2, lines 5-9 of the present application). It is submitted that Dowling discloses memory addressing in connection with program execution by a processor rather than a DMA controller. Therefore, the skilled person would not refer to the teachings of Dowling in order to modify the DMA controller of Heath.

In addition, it is apparent that the address arithmetic units shown in FIG. 2 of Dowling provide only a single address to memory 120 at any time. Address multiplexer 122 provides an address to data memory 120 from register set 102 or from program bus 101, but not two data addresses at the same time. By contrast, the multiplexer recited in Applicant's claim 1 is configured to supply first and second current memory addresses to selected ones of the first and second memory pipelines in response to a control signal. See, for example, MUX 124 in FIG. 2

of the present application. Thus, FIG. 2 of Dowling and the corresponding description do not disclose or suggest a multiplexer as recited by claim 1 and do not disclose or suggest first and second address computation units which permit *DMA transfer of data from one memory space to another memory space* on first and second memory access buses, as required by claim 1.

As noted above, FIG. 6 of Dowling shows a first programmable AAU 617 and a second programmable AAU 619 connected to data memory 658 through address multiplexers 650 and 652, respectively. However, FIG. 6 of Dowling and the accompanying description do not disclose or suggest first and second address computation units which generate addresses at the same time to permit *DMA transfer of data from one memory space to another memory space* on first and second memory access buses, as required by claim 1. Instead, the accessed data words from memory 658 are loaded into registers in register files 632, 634 for operation by the functional units (Col. 17, lines 61-66).

Accordingly, neither Heath nor Dowling discloses first and second address computation units and a multiplexer configured as required by claim 1. For at least these reasons, claim 1 is clearly and patentably distinguished over Heath in view of Dowling, and withdrawal of the rejection is respectfully requested.

Claims 2-8, 25 and 27 depend from claim 1 and are patentable over the cited references for at least the same reasons as claim 1.

Based upon the above discussion, claims 1-8, 25 and 27 are in condition for allowance.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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